



DEPARTMENT OF COMPUTER SCIENCE & DESIGN

Course with Code: Digital Design and Computer Organization (1BCS303)					Faculty: Ms. Bhavana V R			Semester & Section: III	
Module	Class No.	Date planned (DD/MM)	Topics to be covered	TLP Planned	Class No.	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
INTRO	1		Bridge Course						
MODULE-1	2		Introduction: Boolean Algebra and Logic gates						
	3		Basic Theorems And Properties of Boolean Algebra ,Boolean Functions						
	4		Digital Logic Gates						
	5		Integrated Circuits						
	6		Gate-Level Minimization: Introduction, The Map Method						
	7		Four-Variable K-Map						
	8		Four-Variable K-Map						
	9		Product of sums simplification						
	10		Don't-Care Conditions						
	11		NAND Implementation.						
	12		NOR Implementation.						



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MODULE 2	13		Combinational Logic: Introduction,						
	14		Combinational Circuits						
	15		Analysis of Combinational Circuits						
	16		Design Procedure						
	17		Binary Adder						
	18		Binary – Subtractor						
	19		Decoders						
	20		Encoders						
	21		Multiplexers						
	22		Synchronous Sequential Logic: Introduction, Sequential Circuits						
	23		Storage Elements: Latches						
	24		Storage Elements: Flip-Flops						





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MODULE-3	25		Basic Structure of Computers: Functional Units						
	26		Basic Operational Concepts						
	27		Bus structure, Performance – Processor Clock						
	28		Basic Performance Equation, Clock Rate						
	29		Instruction Set: CISC an RISC						
	30		Performance Measurement.						
	31		Machine Instructions and Programs: Memory Location and Addresses,						
	32		Memory Operations						
	33		Instruction and Instruction sequencing						
	34		Addressing Modes.						





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MODULE 4	35		Input/Output Organization: Accessing I/O Devices						
	36		Interrupts – Interrupt Hardware						
	37		Enabling and Disabling Interrupts						
	38		Handling Multiple Devices						
	39		Direct Memory Access						
	40		Buses						
	41		The Memory System: Some Basic Concepts						
	42		Semiconductor RAM Memories						
	43		Read Only Memory						
	44		Speed, size and Cost of memory systems.						
	45		Cache Memories – Mapping Functions.						
	46		Basic Processing Unit: Some Fundamental Concepts						





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MODULE-5	47		Introduction						
	48		Basic Processing Unit: Some Fundamental Concepts						
	49		Execution of a Complete Instruction						
	50		Multiple Bus Organization						
	51		Hardwired Control.						
	52		Hardwired Control.						
	53		Pipelining: Basic concepts						
	54		Role of Cache memory						
	55		Pipeline Performance.						
	56		Revision						





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	Activity	Planned	Actual	Remarks
1	Theory Classes	56		
2	Assignments/ Quizzes/ Self-study	Reflection activity		
3	Tutorials/ Extra classes	-		
4	Internal Assessments	02		
5	ICT based Teaching (% of usage in Curriculum)	100%		
Planning			Execution	
Faculty Signature:			Faculty Signature:	
HoD Signature:			HoD Signature:	

