

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

COURSE MODULE FOR THE SESSION 2026-27 (ODD SEM)

Course Syllabi with CO's

Faculty Name: Roopa B, Dr. Jayant Kumar A Rathod, Dr. Puttegowda D				Academic Year: 2026 - 2027			
Department: Computer Science & Engineering							
Course Code	Course Title	Core / Elective	Prerequisite	Contact			Total Hrs./ Sessions
				Hours			
				L	T	P	
1BCS303	Digital Design & Computer Organization	Core	Basics of Algebra	4	0	0	56 lecture hours + 64 hours of SL&TW
Course Objectives	1. To demonstrate the functionalities of binary logic system 2. To explain the working of combinational and sequential logic system 3. To realize the basic structure of computer system 4. To illustrate the working of I/O operations and processing unit						
Topics Covered as per Syllabus							
Module-1 Boolean Algebra and Logic Gates: Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Digital Logic Gates, Integrated Circuits. Gate-Level Minimization: Introduction, The Map Method, Four-Variable K-Map, Product of sums simplification, Don't-Care Conditions, NAND and NOR Implementation.							
Module-2 Combinational Logic: Introduction, Combinational Circuits, Analysis of Combinational Circuits, Design Procedure, Binary Adder – Subtractor, Decoders, Encoders, Multiplexers. Synchronous Sequential Logic: Introduction, Sequential Circuits, Storage Elements: Latches, Flip-Flops.							
Module-3 Basic Structure of Computers: Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Instruction Set: CISC an RISC, Performance Measurement. Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes.							
Module-4 Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access, Buses. The Memory System: Some Basic Concepts, Semiconductor RAM Memories, Read Only Memory, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions.							

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Module-5

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization. Hardwired Control.

Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.

List of Textbook

1. M. Morris Mano & Michael D. Ciletti, Digital Design, 6th edition, Pearson Education.
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill.

List of Reference books

1. Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning
2. William Stallings: Computer Organization & Architecture, 9th Edition, Pearson, 2015.

Weblinks and Video Lectures (e-Resources)

- NPTEL Video Course: Digital Computer Organization by Prof. P. K. Biswas, IIT Kharagpur - <https://nptel.ac.in/courses/117105078>
2. MIT OpenCourseWare: Computation Structures (6.004) by Prof. Chris Terman, MIT – <https://ocw.mit.edu/courses/6-004-computation-structures-spring-2017/>
3. Computer Organisation Virtual Lab, IIIT Hyderabad (Virtual Labs) – <https://cse11-iiith.vlabs.ac.in/>
4. Infosys Springboard Courses: <https://infyspringboard.onwingspan.com/>

Course Outcomes

At the end of the course the student will be able to:

1. Apply Boolean algebra principles and logic minimization techniques to design and simplify digital logic circuits using logic gates, K-maps, and NAND/NOR implementations.
2. Apply standard design procedures to realize foundational combinational circuits and sequential storage elements.
3. Describe the organization and operation of computer systems, including functional units, bus structures, instruction sets, and addressing modes.
4. Illustrate memory and input/output organization techniques, including interrupts, DMA, cache memory, and semiconductor memory systems.
5. Illustrate the operation of processing units, hardwired control systems, and pipelining techniques to assess computer performance and efficiency
6. Identify computer architecture components, memory organization, and system performance through experimentation and case studies

Assessment Structure:

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the CIE, a student must score at least 40% of 50 marks, i.e., 20 marks.
- To pass the SEE, a student must score at least 35% of 50 marks, i.e., 18 marks.
- Notwithstanding the above, a student is considered to have passed the course, provided the combined total of CIE and SEE is at least 40 out of 100 marks.

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The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)

Subject Code:	1BCS303	TITLE: Digital Design & Computer Organization					Faculty name:		Roopa B, Dr. Jayant Kumar A Rathod, Dr. Puttegowda D			
List of Course Outcomes	Program Outcomes											Total
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	
CO-1	2	3	2	2	2	-	-	2	2	-	1	16
CO-2	2	3	2	2	3	-	-	2	2	-	1	17
CO-3	2	2	1	1	-	-	-	-	-	-	1	7
CO-4	2	2	2	1	-	-	-	-	-	-	1	7
CO-5	2	2	1	1	-	-	-	-	-	-	1	7
CO-6	2	2	2	2	2	-	-	3	3	-	2	18
Total	12	14	10	9	7	-	-	7	7	-	2	72

Note: 3 = Strong Contribution, 2 = Average Contribution, 1 = Weak Contribution, - = No Contribution

The Correlation of Course Outcomes (CO's) and Program Specific Outcomes (PSO's)

Subject Code:	1BCS303	TITLE: Digital Design & Computer Organization		Faculty Name:	Roopa B, Dr. Jayant Kumar A Rathod, Dr. Puttegowda D
List of Course Outcomes	Program Specific Outcomes				Total
	PSO-1		PSO-2		
CO-1	-		-		-
CO-2	-		-		-
CO-3	-		-		-
CO-4	-		-		-
CO-5	-		-		-
CO-6	-		-		-
Total	-		-		-