

DIGITAL DESIGN AND COMPUTER ORGANIZATION

Course Code	1BCS303	Scheme	2025
Type of Course	PCC	Semester	3
Teaching Hours/Week (L:T:P)	4:0:0	CIE Marks	50
Total Hours of Pedagogy per semester L /T/P/SL&TW:	56:0:0:64:120	SEE Marks	50
Credits	4	Total Marks	100
Examination type (SEE)	Theory	Exam Hours	03

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Apply Boolean algebra principles and logic minimization techniques to design and simplify digital logic circuits using logic gates, K-maps, and NAND/NOR implementations.
2. Design combinational and sequential logic circuits using adders, decoders, encoders, multiplexers, latches, and flip-flops.
3. Describe the organization and operation of computer systems, including functional units, bus structures, instruction sets, and addressing modes.
4. Illustrate memory and input/output organization techniques, including interrupts, DMA, cache memory, and semiconductor memory systems.
5. Contrast the operation of processing units, hardwired control systems, and pipelining techniques to assess computer performance and efficiency.
6. Identify computer architecture components, memory organization, and system performance through experimentation and case studies.

SYLLABUS

Module-1

Boolean Algebra and Logic Gates: Basic Theorems And Properties of Boolean Algebra, Boolean Functions, Digital Logic Gates, Integrated Circuits.

Gate-Level Minimization: Introduction, The Map Method, Four-Variable K-Map, Product of sums simplification, Don't-Care Conditions, NAND and NOR Implementation.

Textbook-1: Chapter- 2 (2.4, 2.5, 2.8,2.9), Chapter-3 (3.1, 3.2,3.3,3.4, 3.5,3.6) **Number of Hours: 12**

Module-2

Combinational Logic: Introduction, Combinational Circuits, Analysis of Combinational Circuits, Design Procedure, Binary Adder – Subtractor, Decoders, Encoders, Multiplexers.

Synchronous Sequential Logic: Introduction, Sequential Circuits, Storage Elements: Latches, Flip-Flops.

Textbook-1: Chapter- 4 (4.1, 4.2, 4.3, 4.4, 4.5, 4.9, 4.10, 4.11), Chapter-5 (5.1, 5.2, 5.3, 5.4) **Number of Hours: 12**

Module-3

Basic Structure of Computers: Functional Units, Basic Operational Concepts, Bus structure, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Instruction Set: CISC and RISC, Performance Measurement.

Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes.

Textbook-2: Chapter -1 (1.2, 1.3, 1.4, 1.6), Chapter -2 (2.2, 2.3, 2.4, 2.5) **Number of Hours: 10**

Module-4

Input/Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access, Buses.

The Memory System: Some Basic Concepts, Semiconductor RAM Memories, Read Only Memory, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions.

Textbook-2: Chapter – 4 (4.1, 4.2.1, 4.2.2, 4.2.3, 4.4, 4.5), Chapter-5 (5.1, 5.2, 5.3, 5.4, 5.5.1) **Number of Hours: 12**

Module-5

Basic Processing Unit: Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization. Hardwired Control.

Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.

Textbook-2: Chapter -7 (7.1, 7.2, 7.3, 7.4), Chapter – 8 (8.1) **Number of Hours: 10**

Suggested Learning Resources: (Text Book/ Reference Book/ Manuals):

Textbooks:

1. M. Morris Mano & Michael D. Ciletti, Digital Design, 6th edition, Pearson Education.
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer Organization, 5th Edition, Tata McGraw Hill.

Reference books / Manuals:

1. Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning
2. William Stallings: Computer Organization & Architecture, 9th Edition, Pearson, 2015.

Web links and Video Lectures (e-Resources):

1. NPTEL Video Course: Digital Computer Organization by Prof. P. K. Biswas, IIT Kharagpur - <https://nptel.ac.in/courses/117105078>
2. MIT OpenCourseWare: Computation Structures (6.004) by Prof. Chris Terman, MIT – <https://ocw.mit.edu/courses/6-004-computation-structures-spring-2017/>

3. Computer Organisation Virtual Lab, IIIT Hyderabad (Virtual Labs) – <https://cse11-iiith.vlabs.ac.in/>
4. Infosys Springboard Courses: <https://infyspringboard.onwingspan.com/>

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

- Flipped Classroom
- Problem-Based Learning (PBL)
- Case-Based Teaching
- Simulation and Virtual Labs

Assessment Structure:

The assessment in each course is divided equally between Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE), with each carrying 50% weightage.

- To qualify and become eligible to appear for SEE, in the CIE, a student must score at least 40% of 50 marks, i.e., 20 marks.
- To pass the SEE, a student must score at least 35% of 50 marks, i.e., 18 marks.
- Notwithstanding the above, a student is considered to have passed the course, provided the combined total of CIE and SEE is at least 40 out of 100 marks.

Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]

- A minimum of two Internal Assessment Tests (IA) shall be conducted, carrying a total of 25 marks.
- In addition, Continuous Comprehensive Assessment (CCA) shall be conducted for a total of 25 marks.
- It is recommended to include a maximum of two learning activities as part of the CCA to foster the holistic development of students. These activities shall be:

Sl. No.	Name of the Learning activity	Maximum Marks
1.	Develop Verilog HDL programs for the given problem statement	25

List of Problem Statements:

Sl. No.	Problem Description
1.	Simplify a given 4-variable Boolean expression using appropriate minimization techniques and implement the simplified function using basic logic gates through simulation.
2.	Design and simulate a 4-bit adder–Subtractor circuit using basic logic gates, and verify its functionality for different input combinations.

3.	Design Verilog HDL to implement Binary Adder-Subtractor – Half and Full Adder, Half and Full Subtractor.
4.	Design Verilog program to implement types of De-Multiplexer.
5.	Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D.
6.	Design and implement Verilog programs for SR and JK Flip-Flops. Verify their functionality using simulation.
7.	Identify and document the processor type, clock speed, cache memory, RAM capacity, storage devices, and operating system details of a desktop computer using system information tools.
8.	Observe and record CPU utilization, memory usage, disk activity, and running processes using Task Manager/System Monitor before and after executing multiple applications, and compare the changes in system resource usage.
9.	Measure file transfer rates and access times using desktop computers and discuss their impact on overall system performance and memory hierarchy.
10.	Compare the features, instruction formats, and performance characteristics of CISC and RISC architectures through the study of modern processors, and summarize the findings in a comparative table.
11.	Study of semiconductor RAM and ROM organization with practical examples by determining memory capacity, address lines, data lines, and memory locations, and compare their characteristics.
12.	Identify the major hardware components of a computer system through hands-on inspection, and demonstrate the ability to safely disassemble and reassemble the system while maintaining its functionality.

NOTE: Make use of simulation packages like Xilinx Simulator Interface , Multisim, Modelsim, PSpice or any other relevant. At the end of the course, the students need to submit the report on conduction of the activity with relevant data to the course instructor. Evaluation is for 25 marks.

Rubrics for Learning Activity:

Criteria/ Scale	Superior (5)	Good (4)	Fair (3)	Needs Improvement (2)	Unacceptable (1)
Understanding of Digital Logic / Computer Organization Concepts (CO1, CO2 / PO1, PO2)	Demonstrates complete understanding of the underlying digital logic/ computer organization concepts and correctly explains the design approach.	Demonstrates very good understanding with negligible errors.	Demonstrates adequate understanding with minor misconceptions.	Shows limited understanding and requires guidance.	Unable to understand the concepts.
Circuit Design / Verilog Program Development (CO2, CO3, CO4 / PO2, PO3, PO5)	Designs correct logic circuits/ Verilog programs with efficient implementation and proper coding practices.	Design/ program is correct with minor improvements possible.	Design/ program is mostly correct but contains moderate errors.	Design/ program is partially correct with logical or coding errors.	Unable to develop a functional circuit/ program.
Simulation, Testing and Verification (CO2, CO3, CO4 / PO3, PO4, PO5)	Successfully simulates the design, verifies all test cases, and accurately interprets the results.	Simulation is correct for most cases with minor errors in verification.	Simulation works for standard cases with limited analysis.	Simulation is incomplete or verification contains significant errors.	Unable to simulate or verify the design.
Analysis of Results / Hardware Observation (CO3, CO4, CO5 / PO2, PO4)	Accurately analyzes outputs, compares results, and provides meaningful observations and conclusions.	Good analysis with minor omissions.	Adequate analysis with limited conclusions.	Incomplete analysis and incorrect observations.	No meaningful analysis or conclusions.

Documentation and Record Maintenance (CO3–CO5 / PO2, PO4)	Record is complete, neatly organized, includes circuit diagrams/ programs, simulation outputs, observations, and follows documentation standards.	Well documented with minor formatting issues.	Adequately documented with some missing details.	Poor documentation and incomplete record.	No proper documentation submitted.
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Term Work (TW) and Self Learning (SL) components in Number of Hours per semester

Term work (includes assignments, seminars, micro projects, industrial visits, any other student learning activities etc.)

Sl. No.	Term Work (TW) Activity	Number of Hours / Semester
1.	Learning Activity	30

SL: Self Learning, MOOCs, spoken tutorials, online educational resources etc.

Sl. No.	Self-Learning (SL) Activity	Number of Hours / Semester
1.	Infosys springboard course on: Digital Logic Design Overview	04
2.	Infosys springboard course on: Computer Organization	12
3.	Infosys springboard course on: VLSI Digital Design - Chip Design and Verilog Programming	10
4.	Virtual lab simulation: Computer Organization https://cse11-iiith.vlabs.ac.in OR Simulation Enabled Experiential Learning (SEEL) https://seel.vtu.ac.in/	08

Continuous Internal Evaluation (CIE)

1. The CIE marks shall be decided based on internal tests and other outcome-based activities. The continuous internal evaluation shall be carried out by the teacher handling the course.
2. Out of 50 marks earmarked for CIE, 25 marks shall be assigned for internal tests. The first test shall be conducted after completing two modules of the syllabus and the second one after completing the remaining three modules.

3. The remaining 25 marks shall be assigned for Continuous Course Assessment (CCA), (Learning Activity-Termworks) conducted as per the rubrics listed in the assessment section of the respective syllabus.
4. A student shall obtain a minimum of 40% marks or 20 out of 50 marks allotted to CIE to become eligible to appear for the SEE.

Passing requirement in SEE

1. For a pass in the Semester End Examination (SEE), a student shall secure a minimum of 35 marks out of 100.
2. For the declaration of a pass grade, the sum of the Continuous Internal Evaluation (CIE) marks (out of 50) marks and the SEE marks scaled down to 50 shall be greater than or equal to 40 marks.
3. If the total (CIE + SEE) is less than 40 marks, the student shall be awarded the grade 'F' (Fail).