

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING - CYBER SECURITY

Lesson Plan & Work-done Diary for AY: 2026-27, ODD Semester

Course with Code: Digital Design & Computer Organization -BCS302				Faculty: Prof. Razikha Amreen M I			Semester & Section: III	
Class No.	Date Planned (DD/MM)	Topics to be covered	TLP Planned	Class No.	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-1								
1		Overview of syllabus, Bridge Course	Chalk & Talk	1				
2		Introduction to Digital Design: Binary Logic, Basic Theorems and Properties of Boolean Algebra	PPT	2				
3		Boolean Functions, Digital Logic Gates	Chalk & Talk, PPT	3				
4		Introduction, The Map Method	Chalk & Talk	4				
5		Four-Variable Map	Chalk & Talk	5				
6		Don't-Care Conditions, NAND and NOR Implementation	Chalk & Talk	6				
7		Other Hardware Description Language – Verilog Model of a simple circuit.	Chalk & Talk, PPT	7-8				

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MODULE-2								
1		Combinational Logic: Introduction, Combinational Circuits, Design Procedure	Chalk & Talk, PPT	1				
2		Binary Adder- Subtractor	Chalk & Talk, PPT	2				
3		Decoders, Encoders	Chalk & Talk, PPT	3				
4		Multiplexers	Chalk & Talk, PPT	4				
5		HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder.	PPT	5				
6		Sequential Logic: Introduction, Sequential Circuits	PPT	6				
7		Latches	Chalk & Talk, PPT	7				
8		Flip-Flops	Chalk & Talk, PPT	8				

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MODULE-3								
1		Basic Structure of Computers: Functional Units, Basic Operational Concepts	PPT	1				
2		Bus structure, Performance – Processor Clock	Chalk & Talk, PPT	2				
3		Basic Performance Equation, Clock Rate	Chalk & Talk, PPT	3				
4		Performance Measurement.	Chalk & Talk, PPT	4				
5		Machine Instructions and Programs: Memory Location and Addresses	Chalk & Talk, PPT	5				
6		Memory Operations	Chalk & Talk, PPT	6				
7		Instruction and Instruction sequencing	Chalk & Talk, PPT	7				
8		Addressing Modes.	Chalk & Talk	8				

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MODULE-4								
1		Input/output Organization: Accessing I/O Devices	PPT	1				
2		Interrupts – Interrupt Hardware	PPT	2				
3		Enabling and Disabling Interrupts, Handling Multiple Devices	PPT	3				
4		Direct Memory Access: Bus Arbitration, Speed	PPT	4				
5		Size and Cost of memory systems. Cache Memories – Mapping Functions	PPT	5				
6		Cache Memories – Mapping Functions	PPT/chalk and talk	6				

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MODULE-5								
1		Basic Processing Unit: Some Fundamental Concepts: Register Transfers	PPT	1				
2		Performing ALU operations	PPT	2				
3		fetching a word from Memory, Storing a word in memory.	PPT	3				
4		Execution of a Complete Instruction.	PPT	4				
5		Pipelining: Basic concepts	PPT	5				
6		Role of Cache memory Pipeline Performance.	PPT	6				

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	Activity	Planned	Actual	Remarks
1	Theory Classes	40		
2	Assignments/ Quizzes/ Self-study	2/5		
3	Tutorials/ Extra classes	02		
4	Internal Assessments	03		
5	ICT based Teaching (% of usage in Curriculum)	100%		
Planning			Execution	
Faculty Signature:			Faculty Signature:	
HoD Signature:			HoD Signature:	