

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING - DATA SCIENCE

COURSE MODULE OF THE SUBJECT TAUGHT FOR THE SESSION 2026-27 (ODD SEM)

Course Syllabi with CO's

Faculty Name: Mr. J N Karthik			Academic Year: 2026 - 2027				
Department: Computer Science & Engineering- Data Science							
Course Code	Course Title	Core / Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
1BCS303	Digital Design and Computer Organization	Core	Introduction to Electronics Communication	4	0	0	56T
Course Objectives	1. To demonstrate the functionalities of binary logic system 2. To explain the working of combinational and sequential logic system 3. To realize the basic structure of computer system 4. To illustrate the working of I/O operations and processing unit						
Topics Covered as per Syllabus							
Module-1 Introduction to Digital Design: Binary Logic, Basic Theorems And Properties Of Boolean Algebra, Boolean Functions, Digital Logic Gates, Introduction, The Map Method, Four-Variable Map, Don't-Care Conditions, NAND and NOR Implementation, Other Hardware Description Language – Verilog Model of a simple circuit.							
Module-2 Combinational Logic: Introduction, Combinational Circuits, Design Procedure, Binary Adder-Subtractor, Decoders, Encoders, Multiplexers. HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder. Sequential Logic: Introduction, Sequential Circuits, Storage Elements: Latches, Flip-Flops.							
Module-3 Basic Structure of Computers: Functional Units, Basic Operational Concepts, Bus structure, Performance Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes.							
Module-4 Input/output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access: Bus Arbitration, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions.							
Module-5 Basic Processing Unit: Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory. Execution of a Complete Instruction. Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.							

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List of Textbook and Reference book

1. M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.
2. Carl Hamacher, Zvonko Vranesic, SafwatZaky, Computer Organization, 5 th Edition, Tata McGraw Hill.

Reference books / Manuals:

1. Charles H Roth and Larry L Kinney, Analog and Digital Electronics, Cengage Learning
2. William Stallings: Computer Organization & Architecture, 9th Edition, Pearson, 2015.

Web links and Video Lectures (e-Resources)

<https://cse11-iiith.vlabs.ac.in/>

Course Outcomes

At the end of the course, the student will be able to:

1. CO1: Apply Boolean algebra principles and logic minimization techniques to design and simplify digital logic circuits using logic gates, K-maps, and NAND/NOR implementations.
2. CO2: Design combinational and sequential logic circuits using adders, decoders, encoders, multiplexers, latches, and flip-flops.
3. CO3: Describe the organization and operation of computer systems, including functional units, bus structures, instruction sets, and addressing modes.
4. CO4: Illustrate memory and input/output organization techniques, including interrupts, DMA, cache memory, and semiconductor memory Systems
5. CO5: Contrast the operation of processing units, hardwired control systems, and pipelining techniques to assess computer performance and efficiency
6. CO6: Identify computer architecture components, memory organization, and system performance through experimentation and case studies

Continuous Internal Evaluation CIE [25+25=50 marks]

Continuous Comprehensive Assessments (CCA) 25 Marks + [Internal Assessment(IA): 25 (3 Session Tests are conducted during the semester and

Marks allotted based on average of best two performances)]

Continuous Comprehensive Assessments (CCA)+ Internal Assessment Test (IA) = Continuous Internal Evaluation CIE [25+25=50 marks]

A minimum of **two Internal Assessment Tests (IA)** shall be conducted, carrying a total of **25 marks**.

In addition, **Continuous Comprehensive Assessment (CCA)** shall be conducted for a total of **25 marks**.

It is recommended to include **a maximum of two learning activities** as part of the CCA to foster the **holistic development of students**. These activities shall be:

List of Problem Statements:

NOTE: Make use of simulation packages like Xilinx Simulator Interface , Multisim, Modelsim, PSpice or any other relevant. At the end of the course, the students need to submit the report on conduction of the activity with relevant data to the course instructor. Evaluation is for 25 marks.

Sl. No.	Problem Description
1.	Simplify a given 4-variable Boolean expression using appropriate minimization techniques and implement the simplified function using basic logic gates through simulation.
2.	Design and simulate a 4-bit adder-Subtractor circuit using basic logic gates, and verify its functionality for different input combinations.
3.	Design Verilog HDL to implement Binary Adder-Subtractor – Half and Full Adder, Half and Full Subtractor.
4.	Design Verilog program to implement types of De-Multiplexer.
5.	Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D.

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6.	Design and implement Verilog programs for SR and JK Flip-Flops. Verify their functionality using simulation.
7.	Identify and document the processor type, clock speed, cache memory, RAM capacity, storage devices, and operating system details of a desktop computer using system information tools.
8.	Observe and record CPU utilization, memory usage, disk activity, and running processes using Task Manager/System Monitor before and after executing multiple applications, and compare the changes in system resource usage.
9.	Measure file transfer rates and access times using desktop computers and discuss their impact on overall system performance and memory hierarchy.
10.	Compare the features, instruction formats, and performance characteristics of CISC and RISC architectures through the study of modern processors, and summarize the findings in a comparative table.
11.	Study of semiconductor RAM and ROM organization with practical examples by determining memory capacity, address lines, data lines, and memory locations, and compare their characteristics.
12.	Identify the major hardware components of a computer system through hands-on inspection, and demonstrate the ability to safely disassemble and reassemble the system while maintaining its functionality.

The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)

Course Code:	1BCS303	TITLE: Digital Design and Computer Organization						Faculty Name:	Mr. J N Karthik		
List of Course Outcomes	Program Outcomes										
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11
CO-1	3	-	-	-	3	-	-		3	3	2
CO-2	3	2	2	-	3	-	-	-	3	3	2
CO-3	3	-	-	-	-	-	-	-	-	-	2
CO-4	3	-	-	-	-	-	-	-	-	-	2
CO-5	3	2	-	-	-	-	-	-	-	-	2

Note: 3 = Strong Contribution, 2 = Average Contribution, 1 = Weak Contribution, - = No Contribution

The Correlation of Course Outcomes (CO's) and Program Specific Outcomes (PSO's)

Course Code	1BCS303	Title: Digital Design and Computer Organization	Faculty name: Mr. J N Karthik
List of Course Outcomes	Program Specific Outcomes		
	PSO1	PSO2	
CO1	2	-	
CO2	2	-	
CO3	2	-	
CO4	2	-	
CO5	2	-	

Note: 3 = Strong Contribution, 2 = Average Contribution, 1 = Weak Contribution, - = No Contribution



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