

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE MODULE

Faculty Name: Mr. Pradeep Kumar Y and Mrs. Vineetha S				Academic Year: 2026-27 (ODD Sem)			
Department: ECE							
Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
1BEC302	Digital System Design using Verilog	Core	Number Systems Boolean Algebra Logic gates	3	-	2	40 (8 Hours / Module)
Course objectives: This course will enable students to: 1. Apply Boolean algebra principles to simplify logic functions using Karnaugh Maps (K-Maps) and the Quine–McCluskey minimization technique. 2. Analyze the operation and behavior of combinational logic circuits and standard logic building blocks. 3. Design combinational digital systems using logic gates, multiplexers, decoders, and arithmetic circuits. 4. Analyze and design synchronous and asynchronous sequential circuits using SR, JK, D, and T flip-flops. 5. Model, simulate, and verify combinational and sequential digital circuits using the Verilog Hardware Description Language (HDL).							
Topics Covered as per Syllabus							
MODULE-1							
Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine McCluskey Minimization Technique. Quine McCluskey using Don't CareTerms. (Section 3.1 to3.5 of Text1). RBTL: L1,L2,L3							
MODULE-2							
Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section5.1to5.7 of Text2). RBTL: L1,L2,L3							

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MODULE-3

Flip-Flops and its Applications: The Master-Slave Flip-flops(Pulse-Triggered flip-flops):SR flip flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops.(Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text2). *RBTL: L1,L2,L3*

MODULE-4

Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section1.1to1.6.2, 1.6.4 (only Verilog),2 of Text 3) Verilog Data flow description: Highlights of Data flow description, Structure of Data flow description. (Section2.1to 2.2 (only Verilog) of Text3). *RBTL: L1,L2,L3*

MODULE-5

Verilog Behavioral description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3) Verilog Structural description: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (Section4.1 to 4.2 of Text 3). *RBTL: L1,L2,L3*

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	To simplify the given Boolean expressions and realize using Verilog program
2	To realize Adder/Subtractor(Full/half)circuits using Verilog data flow description.
3	To realize 4-bit ALU using Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a)Gray to binary and vice versa b)Binary to excess3 and vice versa
5	To realize using Verilog Behavioral description:8:1mux, 8:3encoder, Priority encoder
6	To realize using Verilog Behavioral description:1:8Demux, 3:8 decoder,2 –bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a) JK type b) SR type c) T type and d) D type
8	To realize Counters-up/down (BCD and binary)using Verilog Behavioral description.
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.
Open Ended Experiments	
1	Design and Optimization of a Combinational Logic System
2	Configurable Arithmetic Logic Unit (ALU) Design
3	Design of a Finite State Machine (FSM) for a Real-Time Application
4	Sequential Circuit Design Using Flip-Flops
5	Memory-Based System Design Using Verilog Concept

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

List of Text Books

1. Digital Logic Applications and Design by John MYarbrough, Thomson Learning, 2001.
2. Digital Principles and Design by Donald DGivone, McGrawHill, 2002.
3. HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream techpress.

List of Reference Books

1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning.
2. Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007.
3. Fundamentals of HDL, by Cyril PR, Pearson/Sanguine 2010.

List of URLs, Text Books, Notes, Multimedia Content, etc

1. www.chipverify.com
2. <https://www.youtube.com/watch?v=vHLBO05TeyU&list=PLwdnzIV3ogoVIY7iVqrFhWUQEX7JDdiP>
3. <https://www.youtube.com/playlist?list=PLbRMhDVUMngePP5JcezxImF-FzOC9wstz>

Course Outcomes:

At the end of the course the student will be able to:

CO1: Apply Boolean algebra principles to simplify logic functions using Karnaugh Maps (K-Maps) and the Quine–McCluskey minimization technique.	L3
CO2: Analyze the operation and behavior of combinational logic circuits and standard logic building blocks.	L3
CO3: Design combinational digital systems using logic gates, multiplexers, decoders, and arithmetic circuits.	L3
CO4: Analyze and design synchronous and asynchronous sequential circuits using SR, JK, D, and T flip-flops	L3
CO5: Model, simulate, and verify combinational and sequential digital circuits using the Verilog Hardware Description Language (HDL).	L3

The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)

Subject Code: 1BEC302			Title: Digital System Design using Verilog						Faculty Name: Mr. Pradeep Kumar Y and Mrs. Vineetha S			
List of Course Outcomes	Program Outcomes											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	Total
	CO-1	3	3	2	-	-	-	-	-	-	-	8
	CO-2	3	3	2	-	-	-	-	-	-	-	8
	CO-3	3	3	3	-	2	-	-	2	-	-	15
	CO-4	3	3	3	-	2	-	-	2	-	-	15
	CO-5	3	3	3	-	3	-	-	2	-	-	16
Total	15	15	13	-	7	-	-	6	-	-	6	62

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

The Correlation of Course Outcomes (CO's) and Program Specific Outcomes (PSO's)

Subject Code: 1BEC302		TITLE: Digital System Design using Verilog	
List of Course Outcomes	Program Specific Outcomes		
	PSO1	PSO2	Total
CO-1	3	-	3
CO-2	3	-	3
CO-3	3	-	3
CO-4	3	-	3
CO-5	3	-	3
Total	15	-	15

Note: 3 = Strong Contribution 2 = Average Contribution 1 = Weak Contribution - = No Contrib