



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course with Code: Digital System Design Using Verilog (11BEC302)				Faculty:			Semester & Section: 3 rd A and B	
Module	Class No.	Date Planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-1	1		Prerequisites: Number System and Binary addition and Subtraction	Chalk and Talk and PPT				
	2		Prerequisites: Logic Gates, Boolean algebra					
	3		Prerequisites: Verilog Basics					
	4		Principles of Combinational Logic: Definition of combinational logic, Canonical forms					
	5		Generation of switching equations from truth tables					
	6		Karnaugh maps-up to 4 variables					
	7		Karnaugh maps-up to 4 variables with don't care terms					
	8		McCluskey Minimization Technique					
	9		McCluskey Minimization Technique					
	10		McCluskey Minimization Technique with don't care terms & Summary					



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course with Code: Digital System Design Using Verilog (1BEC302)				Faculty: Mr. Pradeep Kumar Y			Semester & Section: 3 rd A and B	
Module	Class No.	Date Planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-2	11		Logic Design with MSI Components and Programmable Logic Devices : Binary Adders and Subtractors	Chalk and Talk and PPT				
	12		Carry look ahead adder					
	13		Comparators and Decoders					
	14		Decoder Example Problems Encoders					
	15		Encoder					
	16		Multiplexers					
	17		Multiplexers example problems					
	18		Programmable Logic Devices(PLDs) Summary and QP discussion					



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course with Code: Digital System Design Using Verilog (1BEC302)				Faculty: Mr. Pradeep Kumar Y			Semester & Section: 3 rd A and B	
Module	Class No.	Date Planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-3	19		Flip-Flops and its Applications: Basics of Flip flop	Chalk and Talk and PPT				
	20		The Master-Slave Flip-flops(Pulse-Triggered flip-flops): SR flip flops, JK flip flops					
	21		Characteristic equations					
	22		Registers					
	23		Binary Ripple Counters, Synchronous Binary Counters					
	24		Counters based on Shift Registers					
	25		Design of Synchronous mod-n Counter using Clocked T, J K, D and SR flip-flops					
	26		Design of Synchronous mod-n Counter using Clocked T, J K, D and SR flip-flops. Summary and QP discussion					



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course with Code: Digital System Design Using Verilog (1BEC302)				Faculty: Mr. Pradeep Kumar Y			Semester & Section: 3 rd A and B	
Module	Class No.	Date Planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-4	27		Introduction to Verilog: Introduction	Chalk and Talk and PPT				
	28		Structure of Verilog module					
	29		Operators, Data Types					
	30		Operators, Data Types					
	31		Styles of Description					
	32		Verilog Data flow description: Highlights of Data flow description					
	33		Structure of Data flow description					
	34		Sample Programs and Summary					



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course with Code: Digital System Design Using Verilog (1BEC302)				Faculty: Mr. Pradeep Kumar Y			Semester & Section: 3 rd A and B	
Module	Class No.	Date Planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-5	35		Verilog Behavioral description: Structure	Chalk and Talk and PPT				
	36		Variable Assignment Statement, Sequential Statements					
	37		Loop Statements					
	38		Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1)					
	39		Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1)					
	40		Verilog Structural description: Highlights of Structural description					
	41		Organization of structural description					
	42		Structural description of ripple carry adder					



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

	Activity	Planned	Actual	Remarks
1	Theory Classes	42		
2	Assignments/Quizzes/ Self-study	3		
3	Tutorials/ Extra classes	-		
4	Internal Assessments	3		
5	ICT based Teaching (% of usage in Curriculum)	70%		
Planning			Execution	
Faculty Signature:			Faculty Signature:	
HOD Signature:			HOD Signature:	