

Digital System Design using Verilog			
Course Code	1BEC302	Scheme	2025
Type of course	Theory and Lab	Semester	III
Teaching Hours/Week (L:T:P)	3:0:2	CIE Marks	50
Total Hours of Pedagogy L:T:P:SL/TW	42:0:28:50	SEE Marks	50
Credits	04	Total Marks	100
Type of Examination (IPCC):	Theory- CIE +SEE, Lab- CIE only.	Exam Hours	3
Course outcome (Course Skill Set) At the end of the course, students will be able to: 1. Apply Boolean algebra principles to simplify logic functions using Karnaugh Maps (K-Maps) and the Quine–McCluskey minimization technique. 2. Analyze the operation and behavior of combinational logic circuits and standard logic building blocks. 3. Design combinational digital systems using logic gates, multiplexers, decoders, and arithmetic circuits. 4. Analyze and design synchronous and asynchronous sequential circuits using SR, JK, D, and T flip-flops. 5. Model, simulate, and verify combinational and sequential digital circuits using the Verilog Hardware Description Language (HDL).			
Module-1			
Principles of Combinational Logic: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text 1). Number of Hours: 08			
Module-2			
Logic Design with MSI Components and Programmable Logic Devices: Binary Adders and Subtractors, Decimal Adders, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2) Number of Hours: 08			
Module-3			
Introduction to Verilog: Structure of Verilog module, Styles of Description, Ports, Operators, Data Types,. (Section 1.1 to 1.6.2 (only Verilog), Text 3) Verilog Data flow description: Highlights of Data flow description, Signal Declaration And Assignment Statement, Structure of Data flow description. (Section 2.1 to 2.2 (only Verilog) of Text 3) Number of Hours: 08			
Module-4			
Flip-Flops and its Applications: The Master-Slave Flip-flops(Pulse-Triggered flip-flops): The basic bistable element, Latches, Timing Considerations, SR flip flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops.(Section 6.1 to 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2) Number of Hours: 10			
Module-5			

	Verilog Behavioral Description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers. (Section 3.1 to 3.4 (only Verilog) of Text 3) Verilog Structural Description: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder.(Section 4.1 to 4.2 of Text 3) Number of Hours: 10
PRACTICAL COMPONENTS OF IPCC	
PART – A: FIXED SET OF EXPERIMENTS	
	1. To simplify the given Boolean expressions and realize using Verilog program 2. To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description. 3. To realize 4-bit ALU using Verilog program. 4. To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess3 and vice versa 5. To realize using Verilog Behavioral description: 8:1mux, 8:3 encoder, Priority encoder 6. To realize using Verilog Behavioral description: 1:8 Demux, 3:8 decoder, 2 –bit Comparator 7. To realize using Verilog Behavioral description: Flip-flops: a)JK type b)SR type c)T type and d) D type 8. To realize Counters-up/down (BCD and binary) using Verilog Behavioral description. 9. Write Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps). 10. Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.
PART – B: OPEN ENDED EXPERIMENTS Open-ended experiments are a type of laboratory activity where the outcome is not predetermined and students are given the freedom to explore, design, and conduct the experiment based on the problem statements as per the concepts defined by the course coordinator. It encourages creativity, critical thinking, and inquiry-based learning.	
	1. Design and Optimization of a Combinational Logic System 2. Configurable Arithmetic Logic Unit (ALU) Design 3. Design of a Finite State Machine (FSM) for a Real-Time Application 4. Sequential Circuit Design Using Flip-Flops 5. Memory-Based System Design Using Verilog Concept
Suggested Learning Resources: (Textbook/ Reference Book/ Manuals): Textbooks: 1. J. M. Yarbrough, Digital Logic Applications and Design. Clifton Park, NY, USA: Thomson Learning, 2006. 2. D. D. Givone, Digital Principles and Design. New York, NY, USA: McGraw-Hill, 2002. 3. N. Botros, HDL with Digital Design: VHDL and Verilog. Dulles, VA, USA: Mercury Learning and Information, 2015 Reference books / Manuals: 1. Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning 2. Fundamentals of HDL, by Cyril PR, Pearson/Sanguine 2010 3. Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007	

Web links and Video Lectures (e-Resources):

1. www.chipverify.com
2. <https://www.youtube.com/watch?v=vHLBO05TeyU&list=PLwdnzlV3ogoVIY7iVqr-FhWUQEX7lDdiP>
3. <https://www.youtube.com/playlist?list=PLbRMhDVUMngePP5lcezxImF-FzOC9wstz>

Teaching-Learning Process (Innovative Delivery Methods):

The following are sample strategies that educators may adopt to enhance the effectiveness of the teaching-learning process and facilitate the achievement of course outcomes.

1. Interactive lectures using digital design visualization tools and multimedia presentations to explain logic design concepts.
2. Simulation-based learning using Verilog HDL simulators to model, simulate, and verify digital circuits.
3. Flipped classroom methodology, where students study digital design concepts before class and engage in design exercises during class.
4. Mini-projects and project-based learning involving the design and verification of digital systems such as counters, ALUs, finite state machines, and controllers.
5. Collaborative learning activities through group discussions, peer reviews, and team-based design projects.
6. Continuous assessment through quizzes, Verilog coding challenges, and design reviews to reinforce learning and provide timely feedback.