

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Lesson Plan & Work-done Diary for AY: 2026-27, ODD Semester

Course with Code: Digital Electronic Circuits / 1BEE304			Faculty: Mrs. Swathi C A			Semester & Section: III	
Class No.	Date planned (DD/MM)	Topics to be covered	TLP Planned	Date of Conduction (DD/MM)	Topics Covered	TLP Executed	Remarks if any deviation
MODULE-1: Principles of Combinational Logic							
1		Definition of combinational logic, Canonical forms	ICT				
2		Generation of switching equations from truth tables, Karnaugh maps- 3,4,5 variables	ICT				
3		Incompletely specified functions (Don 't care terms)	ICT				
4		Simplifying Max term equation	ICT				
5		Quine-McCluskey minimization technique	Chalk & Talk				
6		Quine-McCluskey using don 't care terms	Chalk & Talk				
7		Reduced prime implicants Tables	Chalk & Talk				
8		Design with Basic gates, NAND gates and NOR gates.	Chalk & Talk				

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MODULE-2: Analysis and Design of Combinational logic							
9		General approach to combinational logic design	Chalk & Talk				
10		Decoders and BCD decoders	Chalk & Talk				
11		Encoders	Chalk & Talk				
12		Digital multiplexers	Chalk & Talk				
13		Using multiplexers as Boolean function generators	Chalk & Talk				
14		Adders and subtractors	Chalk & Talk				
15		Cascading full adders	Chalk & Talk				
16		Look ahead carry, Binary comparators	Chalk & Talk				

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MODULE-3: Flip-Flops, Flip-Flops Applications							
17		Basic Bistable elements, Latches, Timing considerations	Chalk & Talk				
18		The master-slave flip-flops	Chalk & Talk				
19		SR flip-flops, JK flip-flops	Chalk & Talk				
20		Edge triggered flip- flops	Chalk & Talk				
21		Characteristic equations	Chalk & Talk				
22		Registers	Chalk & Talk				
23		binary ripple counters, synchronous binary counters	Chalk & Talk				
24		Counters based on shift registers, Design of a synchronous counter	Chalk & Talk				
25		Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.	Chalk & Talk				

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MODULE 4: Sequential systems and Circuit Design							
26		Analysis of Clocked Sequential circuits	Chalk & Talk				
27		State Reduction and Assignment	Chalk & Talk				
28		Design Procedure	Chalk & Talk				
29		Design with State Equations, Sequence detector	Chalk & Talk				
30		Mealy and Moore models	Chalk & Talk				
31		State machine notation	Chalk & Talk				
32		Synchronous Sequential circuit analysis	Chalk & Talk				
33		Construction of state diagrams	Chalk & Talk				
34		counter design	Chalk & Talk				

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		MODULE 5: Memories and Logic Families					
35		Read only and Read/Write Memories	ICT				
36		Programmable ROM	ICT				
37		EPROM	ICT				
38		Flash memory	ICT				
39		Characteristic of Digital ICs, Transistor – Transistor Logic	ICT				
40		Complementary MOS Logic	ICT				
41		Comparison of TTL	ICT				
42		CMOS families	ICT				

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SI No.	Activity	Planned	Actual	Remarks
1	Theory Classes	42		
2	Assignments/Quizzes/ Self study	Quiz – 5 Assessment– 2		
3	Tutorials/ Extra classes	-		
4	Internal Assessments	03		
5	ICT based Teaching (% of usage in Curriculum)	30%		
Planning			Execution	
Faculty Signature:			Faculty Signature:	
HoD Signature:			HoD Signature:	